LISTING OF THE CLAIMS:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Claims 1-34 (Cancelled)

Claim 35 (Withdrawn) A method of forming a planar hybrid-orientation substrate comprising the steps of

forming a bilayer template layer stack comprising a first, lower single crystal semiconductor layer having a first orientation and a second, upper single crystal semiconductor layer having a second orientation different from the first;

amorphizing one of the semiconductor layers of the bilayer template stack in selected areas to form localized amorphized regions; and

recrystallizing the localized amorphized regions using a non-amorphized semiconductor layer of the stack as a template, thereby changing the orientation in the localized amorphized regions from an original orientation to a desired orientation.

Claim 36 (Withdrawn) The method of Claim 35 wherein said first, lower single crystal semiconductor layer is disposed on the insulating layer of an SOI substrate.

Claim 37 (Withdrawn) The method of Claim 35 wherein said first, lower single crystal semiconductor layer comprises a single crystal semiconductor substrate.

Claim 38 (Withdrawn) The method of Claim 35 wherein said second, upper single crystal semiconductor layer is formed atop the first, lower single crystal semiconductor by bonding.

Claim 39 (Withdrawn) The method of Claim 35 wherein said localized amorphized region is formed predominately within the second, upper single crystal semiconductor layer.

Claim 40 (Withdrawn) The method of Claim 35 wherein said localized amorphized region is formed predominately within the first, lower single crystal semiconductor layer.

Claim 41 (Withdrawn) The method of Claim 36 wherein said localized amorphized region is formed predominately within the first, lower single crystal semiconductor layer, and further including the step of removing said top layer after recrystallization, by a process such as chemical mechanical polishing.

Claim 42 (Withdrawn) The method of Claim 35 further comprising forming at least one trench isolation region to separate said areas selected for amorphization from those not selected for amorphization, said at least one trench isolation being formed prior to amorphizing, between amorphizing and recrystallizing, or partially after amorphizing and partially after recrystallizing.

Claim 43 (Withdrawn) The method of Claim 35 wherein said first, lower single crystal semiconductor and layer said second, upper single crystal semiconductor layer are composed of the same or different semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

Claim 44 (Withdrawn) The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer are both composed of a Si-containing semiconductor material.

Claim 45 (Withdrawn) The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer are composed of strained, unstrained or a combination of strained and unstrained semiconductor materials.

Claim 46 (Withdrawn) The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer have different surface orientations selected from (110), (111) and (100).

Claim 47 (Withdrawn) The method of Claim 35 further comprising forming at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

Claim 48 (Withdrawn) The method of Claim 37 further comprising forming a buried insulating layer after said recrystallizing step.

Claim 49 (Withdrawn) The method of Claim 48 wherein said buried insulating layer is formed by a separation-by-ion implantation of oxygen (SIMOX) process.

Claim 50 (Withdrawn) The method of Claim 35 wherein said amorphizing is accomplished by ion implantation.

Claim 51 (Withdrawn) The method of Claim 50 wherein said ion implantation comprises an ion selected from the group consisting of Si, Ge, Ar, C, O, N, H, He, Kr, Xe, P, B and As.

Claim 52 (Withdrawn) The method of Claim 50 wherein said ion implantation comprising an ion selected from the group consisting of Si and Ge.

Claim 53 (Withdrawn) The method of Claim 50 wherein said ion implantation is performed using a patterned mask.

Claim 54 (Withdrawn) The method of Claim 35 wherein said recrystallizing is performed at a temperature from about 200°C to about 1300°C

Claim 55 (Withdrawn) The method of Claim 35 wherein said recrystallizing is performed in a gas selected from the groups consisting of N_2, Ar, He, H_2 and mixtures thereof.

Claim 56 (New) A planar hybrid-orientation semiconductor substrate structure comprising:

at least one clearly defined first single crystal semiconductor region having a first surface crystal orientation, and

at least one clearly defined second single crystal semiconductor region having a second surface crystal orientation different from the first, said second semiconductor regions formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation.

Claim 57 (New) The planar hybrid-orientation substrate structure of Claim 56 further comprising at least one isolation region separating said at least one first single crystal semiconductor region from said at least one second single crystal semiconductor region.

Claim 58 (New) The planar hybrid-orientation substrate structure of Claim 56 further comprising a buried insulator layer, wherein at least some of each first and second semiconductor regions are above said buried insulator layer.

Claim 59 (New) The planar hybrid-orientation substrate structure of Claim 57 wherein said at least one isolation region comprises a dielectric-filled trench.

Claim 60 (New) The planar hybrid-orientation substrate structure of Claim 56 wherein materials of said first and second semiconductor regions are selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

Claim 61 (New) The planar hybrid-orientation substrate structure of Claim 56 wherein said clearly defined first and second single crystal semiconductor regions with different surface orientations both comprise a Si-containing semiconductor material.

Claim 62 (New) The planar hybrid-orientation substrate structure of Claim 56 wherein said at least two clearly defined single crystal semiconductor regions are each comprised of strained, unstrained or a combination of strained and unstrained semiconductor materials.

Claim 63 (New) The planar hybrid-orientation substrate structure of Claim 61 wherein said different surface crystal orientations are selected from the group consisting of (110), (111) and (100).

Claim 64 (New) The planar hybrid-orientation substrate structure of Claim 61 wherein said first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

Claim 65 (New) The planar hybrid-orientation substrate structure of Claim 61 wherein said first Si-containing semiconductor region has a (110) crystal orientation and said second Si-containing semiconductor region has a (100) crystal orientation.

Claim 66 (New) The planar hybrid-orientation substrate structure of Claim 56 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

Claim 67 (New) The planar hybrid-orientation substrate structure of Claim 56 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

Claim 68 (New) The structure of Claim 58 wherein said buried insulator layer is a dielectric material selected from the group consisting of SiO_2, SiO_2 containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials.

Claim 69 (New) A planar hybrid-orientation semiconductor-on-insulator (SOI) substrate structure comprising:

at least one single-layer semiconductor region comprising a semiconductor having a first single-crystal surface orientation, and

at least one bilayer semiconductor region comprising a lower semiconductor layer having said first single-crystal surface orientation and an upper semiconductor layer having a second single-crystal surface orientation different from the first, said single-layer and bilayer semiconductor regions disposed on a buried insulator layer.

Claim 70 (New) The structure of Claim 69 further including at least one isolation region separating said at least one single-layer semiconductor region from said at least one bilayer semiconductor region.

Claim 71 (New) The structure of Claim 69 wherein said isolation region extends down at least to said buried insulating layer.

Claim 72 (New) The structure of Claim 69 wherein said buried insulator layer is a dielectric material selected from the group consisting of SiO_2, SiO_2 containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials.

Claim 73 (New) The planar hybrid-orientation substrate structure of Claim 69 wherein said single-layer and bilayer semiconductor regions both comprise a semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

Claim 74 (New) The structure of Claim 69 wherein said single-layer and bilayer semiconductor regions both comprise a Si-containing semiconductor material.

Claim 75 (New) The structure of Claim 69 wherein said single-layer and bilayer semiconductor regions are each comprised of strained, unstrained or a combination of strained and unstrained semiconductor materials.

Claim 76 (New) The planar-hybrid-orientation SOI substrate structure of Claim 69 further comprising at least one nFET device and at least one pFET device, wherein said at least

one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

Claim 77 (New) The planar hybrid-orientation SOI substrate structure of Claim 69 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

Claim 78 (New) The planar hybrid-orientation SOI substrate structure of Claim 69 wherein first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

Claim 79 (New) The planar hybrid-orientation SOI substrate structure of Claim 69 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

Claim 80 (New) The planar hybrid-orientation SOI substrate structure of Claim 69 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.